

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 1, 8, 13, and 24, as follows:

Listing of Claims:

1. (Currently amended) A memory module, comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface for receiving memory requests for access to at least one of the memory devices;

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices;

a switch for selectively coupling the link interface and the memory device interface;

an I/O register operable to store status information indicative of completion of a DMA operation and error status of the DMA operation; and

a direct memory access (DMA) engine coupled through the switch to the memory device interface, the DMA engine operable to generate generating memory requests for accessing [[to]] at least one of the memory devices to perform DMA operations and further operable to program status information in the I/O register upon completion of the DMA operations.

2. (Original) The memory module of claim 1 wherein the memory hub is an embedded system having the link interface, the memory device interface, the switch, and the DMA engine residing in a single device.

3. (Withdrawn) The memory module of claim 1 wherein the memory device interface comprises:

a memory controller coupled to the switch through a memory controller bus and further coupled to the memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to at least one of the memory devices to which the memory controller is coupled; and

a cache coupled to the memory controller for storing data provided to the memory devices or retrieved from the memory devices.

4. (Original) The memory module of claim 1 wherein the switch comprises a cross-bar switch.

5. (Original) The memory module of claim 1 wherein the plurality of memory devices is a bank of memory devices simultaneously accessed during a memory operation.

6. (Original) The memory module of claim 1 wherein the plurality of memory devices comprise synchronous dynamic random access memory devices.

7. (Original) The memory module of claim 1 wherein the DMA engine comprises:

an address register for storing a starting memory address for a DMA operation;

a target address location for storing a target address of a location to which data is to be moved in the DMA operation;

a count register for storing a count value indicative of the number of memory locations to be accessed in the DMA operation; and

a next register for storing a value representative of the completion of the DMA operation or representative of a memory address corresponding to a link list including a starting memory address, a count value and a next memory address to be loaded into the address register, the count register, and the next register.

8. (Currently amended) A memory hub for a memory module having a plurality of memory devices, comprising:

a link interface for receiving memory requests for access at least one of the memory devices;

a memory device interface for coupling to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices;

a switch for selectively coupling the link interface and the memory device interface;

an I/O register operable to store status information indicative of completion of a DMA operation and error status of the DMA operation; and

a direct memory access (DMA) engine coupled through the switch to the memory device interface, the DMA engine operable to generate generating memory requests for accessing [[to]] at least one of the memory devices to perform DMA operations and further operable to program status information in the I/O register upon completion of the DMA operations.

9. (Original) The memory hub of claim 8 wherein the link interface, the memory device interface, the switch, and the DMA engine are embedded systems residing in a single device.

10. (Withdrawn) The memory hub of claim 8 wherein the memory device interface comprises:

a memory controller coupled to the switch through a memory controller bus and further coupled to the memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to at least one of the memory devices to which the memory controller is coupled; and

a cache coupled to the memory controller for storing data provided to the memory devices or retrieved from the memory devices.

11. (Original) The memory hub of claim 8 wherein the switch comprises a cross-bar switch.

12. (Original) The memory hub of claim 8 wherein the DMA engine comprises:

an address register for storing a starting memory address for a DMA operation;

a target address location for storing a target address of a location to which data is to be moved in the DMA operation;

a count register for storing a count value indicative of the number of memory locations to be accessed in the DMA operation; and

a next register for storing a value representative of the completion of the DMA operation or representative of a memory address corresponding to a link list including a starting memory address, a count value and a next memory address to be loaded into the address register, the count register, and the next register.

13. (Currently amended) A memory system, comprising:

a memory bus on which memory requests are provided; and

a plurality of at least one memory modules coupled to the memory bus, each [[the]] memory module having a plurality of memory devices and a memory hub, the memory hub comprising:

a link interface coupled to receive memory requests for access to at least one of the memory devices of the memory module on which the link interface is located;

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices;

a switch for selectively coupling the link interface and the memory device interface;

an I/O register operable to store status information indicative of completion of a DMA operation and error status of the DMA operation; and

a direct memory access (DMA) engine coupled through the switch to the memory device interface and the link interface, the DMA engine operable to generate generating memory requests for accessing [[to]] at least one of the memory devices to perform DMA operations and further operable to program status information in the I/O register upon completion of the DMA operations.

14. (Original) The memory system of claim 13 wherein the memory hub is an embedded system having the link interface, the memory device interface, the switch, and the DMA engine residing in a single device.

15. (Original) The memory system of claim 13 wherein the memory bus comprises a high-speed memory bus.

16. (Original) The memory system of claim 13 wherein the memory bus comprises a high-speed optical memory bus and wherein the link interface comprises an optical memory bus interface circuit for translating optical signals and electrical signals.

17. (Original) The memory system of claim 13 wherein a plurality of memory modules are included in the memory system and a first memory module of the plurality of memory modules is coupled to the memory bus and the remaining memory modules of the plurality are coupled in series with the first memory module.

18. (Original) The memory system of claim 13 wherein a plurality of memory modules are included in the memory system and each of the plurality of memory modules are coupled directly to the memory bus through a respective link interface.

19. (Withdrawn) The memory system of claim 13 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the switch through a memory controller bus and further coupled to the memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to at least one of the memory devices to which the memory controller is coupled; and

a cache coupled to the memory controller for storing data provided to the memory devices or retrieved from the memory devices.

20. (Original) The memory system of claim 13 wherein the switch of the memory hub comprises a cross-bar switch.

21. (Original) The memory system of claim 13 wherein the plurality of memory devices of a memory module represents a bank of memory devices simultaneously accessed during a memory operation.

22. (Original) The memory system of claim 13 wherein the plurality of memory devices of the memory modules comprise synchronous dynamic random access memory devices.

23. (Original) The memory system of claim 13 wherein the DMA engine of the memory hub comprises:

an address register for storing a starting memory address of a memory location in the memory system at which a DMA operation begins;

a target address location for storing a target address of a memory location in the memory system to which data is to be moved in the DMA operation;

a count register for storing a count value indicative of the number of memory locations to be accessed in the DMA operation; and

a next register for storing a value representative of the completion of the DMA operation or representative of a memory address corresponding to a link list including a starting memory address, a count value and a next memory address to be loaded into the address register, the count register, and the next register.

24. (Currently amended) A computer system, comprising:

- a central processing unit (“CPU”);
- a system controller coupled to the CPU, the system controller having an input port and an output port;
- an input device coupled to the CPU through the system controller;
- an output device coupled to the CPU through the system controller;
- a storage device coupled to the CPU through the system controller;
- a plurality of at least one memory modules, each [[the]] memory module comprising:
 - a plurality of memory devices; and
 - a memory hub, comprising:
 - a link interface coupled to receive memory requests for access to at least one of the memory devices of the memory module on which the link interface is located;
 - a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices;
 - a switch for selectively coupling the link interface and the memory device interface;
 - an I/O register operable to store status information indicative of completion of a DMA operation and error status of the DMA operation; and
 - a direct memory access (DMA) engine coupled through the switch to the memory device interface and the link interface, the DMA engine operable to generate generating memory requests for accessing [[to]] at least one of the memory devices of the plurality of memory modules to perform DMA operations and further operable to program status information in the I/O register upon completion of the DMA operations; and
 - a communications link coupled between the system controller and ~~at least one of~~ the plurality of memory modules for coupling memory requests and data between the system controller and the memory modules.

25. (Original) The computer system of claim 24 wherein the communications link comprises a high-speed memory bus.

26. (Original) The computer system of claim 24 wherein the memory hub is an embedded system having the link interface, the memory device interface, the switch, and the DMA engine residing in a single device.

27. (Original) The computer system claim 24 wherein the communications link comprises a high-speed optical memory bus and wherein the link interface of the memory hub comprises an optical memory bus interface circuit for translating optical signals and electrical signals.

28. (Original) The computer system of claim 24 wherein a plurality of memory modules are included in the computer system and a first memory module of the plurality of memory modules is coupled to the communications link and the remaining memory modules of the plurality are coupled in series with the first memory module.

29. (Original) The computer system of claim 24 wherein a plurality of memory modules are included in the computer system and each of the plurality of memory modules are coupled directly to the memory bus through a respective link interface.

30. (Withdrawn) The computer system of claim 24 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the switch through a memory controller bus and further coupled to the memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to at least one of the memory devices to which the memory controller is coupled; and

a cache coupled to the memory controller for storing data provided to the memory devices or retrieved from the memory devices.

31. (Original) The computer system of claim 24 wherein the switch of the memory hub comprises a cross-bar switch.

32. (Original) The computer system of claim 24 wherein the plurality of memory devices of a memory module represents a bank of memory devices simultaneously accessed during a memory operation.

33. (Original) The computer system of claim 24 wherein the plurality of memory devices of the memory module comprise synchronous dynamic random access memory devices.

34. (Original) The computer system of claim 24 wherein the DMA engine of the memory hub comprises:

an address register for storing a starting memory address of a memory location in the memory system at which a DMA operation begins;

a target address location for storing a target address of a memory location in the memory system to which data is to be moved in the DMA operation;

a count register for storing a count value indicative of the number of memory locations to be accessed in the DMA operation; and

a next register for storing a value representative of the completion of the DMA operation or representative of a memory address corresponding to a link list including a starting memory address, a count value and a next memory address to be loaded into the address register, the count register, and the next register.

35-42. (Cancelled)